REMARKS

In accordance with the foregoing, various of the claims have been amended to improve form and to establish proper antecedent support. No new matter is presented. Accordingly, approval and entry of the foregoing claim amendments are respectfully requested.

The FINAL Office Action mailed November 18, 2003 herein sets forth the Examiner's Remarks at pages 2-5, addressing the arguments filed by applicants herein on August 27, 2003, the headings as to specific sections of the Remarks and claims to which those Remarks relate, at pages 2-5, being repeated in the following.

The CLAIM REJECTIONS from pages 5-20 correspond substantially to the Claim Rejections of the non-final Office Action mailed May 23, 2003, pages 2-12 although expanded to encompass claims newly added in the intervening response and, accordingly, applicants, in response thereto, incorporate by reference herein the Amendment and Remarks filed May 23, 2003.

CLAIMS 1, 9, 17 AND 71

With regard to claims 1, 9, 17 and 71, the Examiner maintains his contentions that Katayama et al. discloses only a single power distribution circuit comprising MOSFETs 10, 11 and a controller. However, Katayama et al. does not disclose the features that a power distribution circuit is connected between a high potential power supply line and a driving device without providing another power distributing circuit between a low potential power supply line and the driving device (claims 1 and 17), and that a power distribution circuit is connected between the low potential power supply line and the driving device without providing another power distributing circuit between the high potential power supply line and the driving device (claims 9 and 71). Specifically, in Katayama et al., a first power distribution circuit 10 (12) is connected between a high potential power supply line (+) and a driving device, and further a second power distribution circuit 11 (13) is connected between a low potential power supply line (-) and the driving device.

Note further that Katayama et al. describes, in col. 4, lines 41-44: "Therefore, the temperature rise in the driver IC 5 is suppressed, and the operation of the driver IC 5 is stabilized, only by using two outside resistors 12 and 13." Further, in Katayama et al, if a pair of power distributing circuits are not provided at both plus and minus terminals of the power source 9, temperature increases of the P-channel LDMOS 7 and the N-channel LDMOS 8 are

not balanced and the operation of the driver IC 5 is not stabilized. Therefore, Katayama et al. does not teach or suggest the above special features of claims 1, 9, 17, and 71.

CLAIMS 35, 65 AND 68

With regard to claims 35, 65, and 68, the Examiner points out in the present Office Action that a resistance of the resistors 12, 13 must be very high in order to apply high voltage. However, as described in col. 4, lines 29 through 44 of Katayama et al., the resistance values of the resistors 12 and 13 do not depend on the voltage of the power source 9, and the resistance values of the resistors 12 and 13 must be designed by considering a ratio of the resistance values of the resistors 12, 13 and resistive impedances of LDMOSs (driving devices) 7, 8. When an output voltage of the power source 9 becomes high and a high voltage driving pulse is required, a large amplitude pulse signal without having distortion can be applied to a capacitive load by increasing currents flowing through the resistors 12, 13.

Incidentally, when driving a capacitive load CL while a gate input signal is quickly applied, if conductive resistances of output transistors or MOSFETs and a series combined resistance R of the resistors 12, 13 are not designed to sufficiently low values, rising and falling transient times of an output driving pulse become long, so that it becomes difficult to drive the capacitive load. Therefore, so as to obtain a high speed pulse required for driving the capacitive load, the resistance value R of the resistors 12, 13 must be designed to be lower than a specific resistance value determined by the relationship of the capacitive load and the rising and falling transient times, regardless the driving voltage value. Specifically, in Katayama et al., the resistors 12, 13 must be low values so as to apply the high voltage at a high speed during a short switching period for each element and, therefore, there is no teaching or suggestion that the power distributing circuit is a resistive element having an impedance whose value is not smaller than one-tenth of the value of a resistive component of a conducting impedance of a driving device.

Amended claim 35 recites the feature that "the resistive impedance is inserted between the output terminal and the capacitive load" is included; claim 65 recites the features that "a power distributing circuit is connected between the high potential power supply line and the driving device" and "the power distributing circuit is a resistive element having an impedance whose value is not smaller than one-tenth of the value of a resistive component of the conducting impedance of the driving device"; and claim 68 recites the features that "a power distributing circuit is connected between the low potential power supply line and the driving

device" and "the power distributing circuit is a resistive element having an impedance whose value is not smaller than one-tenth of the value of a resistive component of the conducting impedance of the driving device"--which are submitted to clarify the differences between the present invention, as recited in these claims 35, 65, and 68, and Katayama et al.

Further, in claims 65 and 68, an interference avoiding device, which is used to suppress an excess drive current flowing into the capacitive load, is connected in series between the power distributing circuit and the output terminal. Please note that the interference avoiding device corresponds to, for example, a series-connected diode 60 or 70 in Fig. 13, and by eliminating unnecessary output voltage variations using the series-connected diode 60 or 70, it becomes possible to suppress an excess drive current flowing into the load capacitor due to the interference occurring between the outputs via a common power supply line or a reference potential line connected to ground, so that the power consumption of the driving circuit 3 can be reduced. Katayama et al. does not teach or suggest the above special characteristics of the present invention, as recited in claims 65 and 68.

CLAIMS 66 AND 69

In claim 66, the features "a power distributing circuit is connected between the high potential power supply line and the driving device" and "the power distributing circuit is constant-current source" are included; in claim 69, the features 11a power distributing circuit is connected between the low potential power supply line and the driving device" and "the power distributing circuit is a constant-current source" are included.

In Katayama et al., a current i flowing through the resistors 12, 13 or power MOSFETs 10, 11 is described by the following equation:

$$i=Imax \times \exp(-t/(CL \times R))$$

where, t is a progressing time from a pulse edge.

Specifically, a transitional current i is exponentially decreased in response to the progressing time t. In this state (i.e., during the time when transitional current i is flowing), a ratio between the voltage drop caused by the resistors 12, 13 and the voltage drop caused by the drive elements 7, 8 is maintained at a constant value since both resistors 12, 13 and drive elements 7, 8 are positioned in the same circuit load where the current i is flowing and, therefore, instantaneous and average power consumption is distributed in the resistors 12, 13 and the drive elements 7, 8 according to the ratio.

On the other hand, in the present invention as recited in claims 66 and 69, the above resistors 12, 13 and power MOSFETs 10, 11 are replaced by a constant-current source for regulating the current i at a constant value and, therefore, almost all voltage drop and power consumption occur at the power distributing circuit; therefore, the temperature rise (power consumption) of drive elements is distributed. Therefore, Katayama et al. does not teach or suggest the above special features of claims 66 and 69.

CLAIMS 67 AND 70

With regard to claims 67 and 70, as described above, and similarly to claims 65 and 68, an interference avoiding device is connected in series between the power distributing circuit and the output terminal. Katayama et al. does not teach or suggest the above special characteristics of the present invention, as recited in claims 67 and 70.

With regard to Miyazaki, as shown in Fig. 4(a) (and Fig. 4(b)) thereof, a gate terminal of MOS transistor MN3 (MN6) having high input impedance characteristics is connected to an input terminal IN of each of plural driving devices (amplifiers) A1 to A5; therefore, a current (power) passing through resistors R1 to R5 does not flow. Further, as is apparent in the description explaining Fig. 1 (col. 6, lines 38 through 45), the values of resistors R1 through R5 are selected in the range of several tens of kilohms to several hundreds of kilohms (i.e., very high resistance values) to avoid any flow of wasteful, idling current.

Applicants respectfully submit that it is impossible to supply power via these resistors R1 through R5. Specifically, in Miyazaki, the buffer amplifiers A1 through A5 receive the divided voltage levels and drive the liquid crystal load. In Miyazaki, the resistors R1 through R5 do not have a power supplying ability to supply power to the buffer amplifiers (driving devices) A1 through A5. Therefore, Miyazaki is basically different from the present invention.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that the pending claims patentably distinguish over the references of record, taken singly or in any proper combination and, further, there being no other objections or rejections, that the application is in condition for allowance, which action is earnestly solicited.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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